

ATTORNEY DOCKET NO. 97-C-108 (STMI01-97108)
U.S. SERIAL NO. 09/160,824
PATENT

REMARKS

Claims 1-20 are pending in the present application. Claim 20 was withdrawn from consideration as directed to a non-elected species.

Reconsideration of the claims is respectfully requested.

35 U.S.C. § 112, First Paragraph (Written Description)

Claims 7 and 9 were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter not which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time of the application was filed, had possession of the claimed invention. This rejection is respectfully traversed.

The Office Action asserts that the limitation of "contact pads on the active surface of the first integrated circuit chip for external connection to the central processing unit" is not supported by the original disclosure. However, the specification as filed depicts such pads 20 in Figures 1 and 2, and also contains a description of such pads:

... Finally, disposed on the same surface of the integrated circuit chip 12 as the electrical contacts 16, are pads 20 that serve to connect the integrated circuit microprocessor 10 with a mother or sister-board.

Figure 2 is a cross-sectional side view of an integrated circuit microprocessor 10 made in accordance with the present invention. In order to provide for the electrical connection of the integrated circuit microprocessor 10, the pads 20 are located so as to permit the deposition of solder balls, solder columns or connection by wire bonding for connection with, e.g., a printed circuit board such as a mother or sister board.

Specification, page 13, lines 7-19.

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Therefore, the rejection of claims 7 and 9 under 35 U.S.C. § 112, first paragraph has been overcome.

35 U.S.C. § 102 (Anticipation)

Claims 1, 3-4, 6, 8, 10-11, 13-14, 16 and 18 were rejected under 35 U.S.C. § 102(a) as being anticipated by U.S. Patent No. 5,677,567 to *Ma et al.* This rejection is respectfully traversed.

As previously noted, independent claims 1 and 13 each recite that the second (integrated circuit) chip is mounted on the active face of the first (integrated circuit) chip. Such a feature is not shown or suggested by the cited reference. The cited portion of *Ma et al* discloses integrated circuits 702 and 704/706 mounted on opposite sides of a single lead frame die paddle 708. *Ma et al* does not teach or suggest mounting one integrated circuit on the active surface of another integrated circuit.

The final Office Action fixes on the use of the term "directly" in the response to the previous and the absence of that term from the claims. However, Applicants respectfully note that the claims recite that the chip is mounted "on" the active face, where the term "on" is normally interpreted as requiring direct contact, as opposed to reciting that the chip is mounted "over" the active face, where the claim term "over" is normally interpreted as permitting intervening layers. Thus, the claim limitation of the second chip being "on" the active surface of

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another integrated circuit is not shown or suggested by *Ma et al*, since *Ma et al* only discloses integrated circuits which are "on" opposite faces of a lead frame.

In addition, claim 11 recites direct connection of the metal regions on the active faces of the first and second integrated circuit chips by a bonding layer. The lead frame of *Ma et al* is not a bonding layer.

Claim 7 recites that the distance between active faces of the two integrated circuits is sufficient to permit electrical connection to contact pads on the active surface of one integrated circuit for external connection thereto. Such a feature is not shown or suggested by *Ma et al*.

Claim 9 recites that the second integrated circuit chip has a width less than a distance between two groups of contact pads on the active surface of the first integrated circuit chip. Such a feature is not shown or suggested by *Ma et al*.

Claims 10 and 18 recite that a third integrated circuit is also mounted on an active face of the first integrated circuit, adjacent to the second integrated circuit. Such a feature is not shown or suggested by *Ma et al*. *Ma et al* depicts, in Figure 7, two integrated circuits 704 and 706 mounted on one side of a lead frame 708 and a third integrated circuit 702 mounted on the opposite side of the lead frame 708. While integrated circuits 704 and 706 are adjacent, they are not "on" integrated circuit 702.

Claim 12 recites that the length and width of the second integrated circuit chip are less than a respective length and width of the first integrated circuit chip. Claim 19 similarly recites

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that the width of the second integrated circuit chip is less than the width of the first integrated circuit chip. Such a feature is not shown or suggested by *Ma et al.*

Claim 14 recites insulating regions projecting from the active faces of the first and second chips covered by conductive layers. Such a feature is not shown or suggested by *Ma et al.*

Therefore, the rejection of claims 1, 3-4, 6, 8, 10-11, 13-14, 16 and 18 under 35 U.S.C. § 102 has been overcome.

35 U.S.C. § 103 (Obviousness)

Claims 2, 5, 15 and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ma et al.* Claims 12 and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ma et al.* in view of U.S. Patent No. 5,869,895 to *Raad*. These rejections are respectfully traversed.

As previously noted, *Raad*, like *Ma et al.*, teaches mounting memory device 103 on an electrical contact frame 109, which is in turn mounted "adjacent to the top surface 107" of a microprocessor 101 in contact with electrical contact pads 105 projecting from the surface of microprocessor 101. Accordingly, neither reference teaches or suggested mounting an integrated circuit on the active face of another integrated circuit.

Therefore, the rejection of claims 2, 5, 12, 15 and 19 under 35 U.S.C. § 103 has been overcome.

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SUMMARY

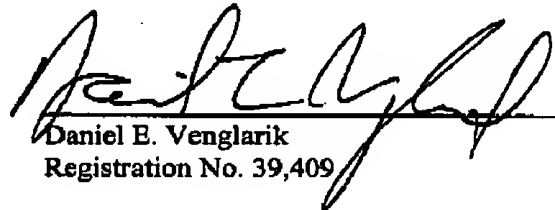
For the reasons given above, the Applicant respectfully requests reconsideration and allowance of pending claims and that this Application be passed to issue. If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at dvenglarik@davismunck.com.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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